We claim:

1. A method of forming dual gate dielectric layers on a substrate comprising:

(a) providing a substrate with isolation regions that separate device areas;

(b) depositing an interfacial layer on said substrate;

(c) depositing a high k dielectric stack on said interfacial layer;

(d) removing the interfacial layer and high k dielectric stack over one device area; and

(e) growing a second dielectric layer on the exposed device area, said growth simultaneously anneals said high k dielectric layer.

2. The method of claim **1** wherein the isolation regions are shallow trench isolation features in a silicon substrate.

3. The method of claim **1** wherein the interfacial layer is comprised of silicon oxynitride, SiO_2, or silicon nitride with a thickness between about 1 and 30 Angstroms.

4. The method of claim **1** wherein the interfacial layer is omitted and the high k dielectric stack is deposited on the substrate.

5. The method of claim **1** wherein the high k dielectric stack is deposited to a thickness from about 15 to 100 Angstroms.

6. The method of claim **1** wherein the high k dielectric stack is comprised of a high k dielectric material selected from the group including Ta_2O_5, TiO_2, Al_2O_3, ZrO_2, HfO_2, Y_2O_3, L_2O_3 and their aluminates and silicates.

7. The method of claim **6** wherein the high k dielectric stack is comprised of two or more layers comprised of one or more of said high k dielectric materials.

8. The method of claim **1** wherein a photoresist is patterned on said high k dielectric layer and serves as an etch mask for selectively removing the interfacial layer and high k dielectric layer over one device area.

9. The method of claim **8** further comprising stripping said photoresist and cleaning the substrate after said etch process is complete.

10. The method of claim **1** wherein said second dielectric layer that is grown on the exposed device area is comprised of SiO_2 or silicon oxynitride preferably with an effective oxide thickness (EOT) of < 10 nm.

11. The method of claim **1** wherein said interfacial layer and second dielectric layer are formed by a rapid thermal process in a temperature range of about 500^{O}C to 1000^{O}C for a period of about 10 to 500 seconds.

12. The method of claim **1** further comprising the steps of depositing a conductive layer following the high k dielectric anneal, forming a gate electrode in each device area, adding spacers on the sidewalls of the gate electrode, dielectric layers, and interfacial layer, forming source/drain regions, and forming contacts to the gate electrodes and to source/drain regions to complete the MOSFET devices.

13. The method of claim **12** wherein the resulting MOSFET containing the high k dielectric stack is a low power device and the MOSFET containing the oxide or oxynitride dielectric layer is a high performance device.

14. The method of claim **11** wherein a high k dielectric stack comprised of ZrO_2 and Al_2O_3 is subjected to a post-deposition anneal during the growth of a second dielectric layer comprising SiON, said anneal involving NH_3 which further reduces the leakage current and lowers the EOT in the resulting device.

15. The method of claim **11** wherein a high k dielectric stack comprised of HfO_2 is subjected to a post-deposition anneal during the growth of a second dielectric layer comprising SiO_2, said anneal involving O_2 which further reduces leakage current in the resulting device.

16. A method of forming triple gate dielectric layers on a substrate comprising:

(a) providing a substrate with isolation regions that separate a first, second, and third device area;

(b) depositing an interfacial layer on said substrate;

(c) depositing a high k dielectric stack on said interfacial layer;

(d) removing the interfacial layer and high k dielectric stack over said second and third device areas;

(e) growing a second dielectric layer on the exposed second and third device areas;

(f) removing the second dielectric layer over said third device area; and

(h) growing a third dielectric layer on the exposed third device area, said growth simultaneously anneals said high k dielectric stack.

17. The method of claim **16** wherein the isolation regions are shallow trench isolation features in a silicon substrate.

18. The method of claim **16** wherein the interfacial layer is comprised of silicon oxynitride, SiO_2, or silicon nitride with a thickness between about 1 and 30 Angstroms.

19. The method of claim **16** wherein the interfacial layer is omitted and the high k dielectric stack is deposited on the substrate.

20. The method of claim **16** wherein the high k dielectric stack is deposited to a thickness of about 15 to 100 Angstroms.

21. The method of claim **16** wherein the high k dielectric stack is comprised of a high k dielectric material selected from the group includingTa_2O_5, TiO_2, Al_2O_3, ZrO_2, HfO_2, Y_2O_3, L_2O_3 and their aluminates and silicates.

22. The method of claim **21** wherein the high k dielectric stack is comprised of two or more layers comprised of one or more of said high k dielectric materials.

23. The method of claim **16** wherein removing one or more layers above one or more device areas comprises patterning a photoresist and using said pattern as an etch mask while undesired layers are etched away.

24. The method of claim **23** further comprised of stripping said photoresist and cleaning the substrate after said etch process is complete.

25. The method of claim **16** wherein a dielectric layer comprised of SiO_2 or silicon oxynitride with an effective oxide thickness (EOT) of < 10 nm is deposited as the second dielectric layer and SiO_2 with a thickness in the range of 10 to 100 Angstroms is deposited as the third dielectric layer.

26. The method of claim **16** wherein the high k dielectric stack is annealed during said growth of said second dielectric layer on the exposed device areas.

27. The method of claim **16** wherein said interfacial layer and second and third dielectric layers are formed by a rapid thermal process in a temperature range of about $500^{o}C$ to $1000^{o}C$ for a period of about 10 to 500 seconds

28. The method of claim **16** further comprising the steps of depositing a conductive layer following deposition of the third dielectric layer, forming a gate electrode in each device area, adding spacers to the gate electrodes, forming source/drain regions, and forming silicide regions on said gate electrodes and on the source/drain regions to form MOSFET devices.

29. The method of claim **28** wherein the resulting MOSFET containing the high k dielectric stack is a low power device, the MOSFET containing the second dielectric layer is a high performance device, and the MOSFET containing the third dielectric layer is an I/O device.

30. The method of claim **26** wherein a high k dielectric stack comprised of ZrO_2 and Al_2O_3 is subjected to a post-deposition anneal during growth of a second dielectric layer comprising SiON, said anneal involving NH_3 which further reduces the leakage current and lowers the EOT in the resulting device.

31. The method of claim **26** wherein a high k dielectric stack comprised of HfO_2 is subjected to a post-deposition anneal during the growth of a second dielectric layer comprising SiO_2, said anneal involving O_2 which further reduces leakage current in the resulting device.